DESIGN OF AN ADVANCED MODULAR AUTOMATED EVALUATION SYSTEM FOR EXPERIMENTAL HIGH POWER SGTOS

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Abstract

An advanced evaluation system for experimental high power Super Gate Turn Off Thyristors (SGTOs) with built – in custom data acquisition and characterization electronics was designed and built in a cooperative agreement between engineers at Texas Tech University's Center for Pulsed Power and Power electronics (P^3E) laboratory and research scientists at Army Research Lab (ARL). The system consist of a Pulse Forming Network (PFN) energized by a rapid capacitor charger, a data acquisition system which records chosen waveforms for each test cycle and a curve tracing module which the test devices are mechanically switched into to record current and voltage characteristics at arbitrary intervals between high power cycles. Testing is completely automated, with all test parameters including charge level, repetition rate, volume, etc. set within a windows based GUI. The evaluation system has successfully recorded changing I – V characteristics before actual physical failure in several devices. Extremely high volume testing has also been carried out with one device having been cycled over 42,000 times at moderate (2.5 kA) conduction levels.

I. INTRODUCTION

In the ongoing effort to improve high power solid state switching elements, new structural designs for Si switches, as well as newer wide band – gap materials like SiC and GaN, have produced solid state control elements that are capable of hold off voltages and current conduction levels previously unattainable with prior semiconductor designs. While any increase in current capacity or hold off voltage in a solid state device is an attractive proposition, the design of any new semiconductor switch is a complex proposition, and no matter how well thought out, the actual physical implementation must be thoroughly evaluated before being placed in an application where failure could possibly have catastrophic consequences. Stressing new device designs in high energy test platforms is quite common, with the goal of finding at what levels failure happens. It is not adequate, however to simply note failure at a given energy level; understanding why or in what manner failure occurs is crucial in the evolution of any given device. To achieve a clearer picture of device failure, voltage and current waveforms for every test cycle must be captured and perhaps even more importantly, device characterization needs to be carried out frequently to provide a glimpse of the true reason any particular device fails. Unfortunately, there is an inherent trade – off between sheer volume of data recorded and the number and time between test cycles, and characterizing a device requires physically removing it from a test bed. To circumvent these obstacles and provide a reliable temporal view of both device performance under operating conditions and device characteristics, Texas Tech University's Center for Pulsed Power and Power Electronics (P^3E) lab working in conjunction with Army Research Lab (ARL) developed a completely automated, modular test bed that runs an arbitrary number of cycles while recording all pertinent waveforms with a proprietary oscilloscope and at regular settable intervals switches the Device Under Test (DUT) out of the test bed's high energy section via a custom electromechanical switch into a fast characterization module to record any changes in I – V curves.

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II. DEVICE(S) UNDER TEST

The test bed was designed specifically to characterize two distinctly different SGTO architectures: a Si based design manufactured by Silicon Power Corporation and a 4H – SiC device from Cree, Inc. Figure 1 displays packaged versions of each type along with nominal ratings and triggering methods. Earlier generations of these SGTOs have been evaluated with manual test beds and wide – pulse, low current protocols [1 – 2].

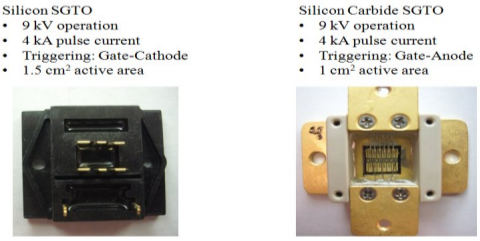

Figure 1. Si and SiC SGTOs

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14. ABSTRACT
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III. SYSTEM DESCRIPTION

Figure 2 is a simplified block diagram of the complete system. The automated test bed carries out a user settable test sequence configured within a windows GUI on a host computer while recording desired voltage and current signals in the form of both image files and raw data (.CSV) files. At arbitrary intervals, the DUT is switched out of the high energy path and connected to a fast characterization module which produces I – V curves that are also uploaded to the host computer. The DUT is then returned to the high energy section for repetitive testing.

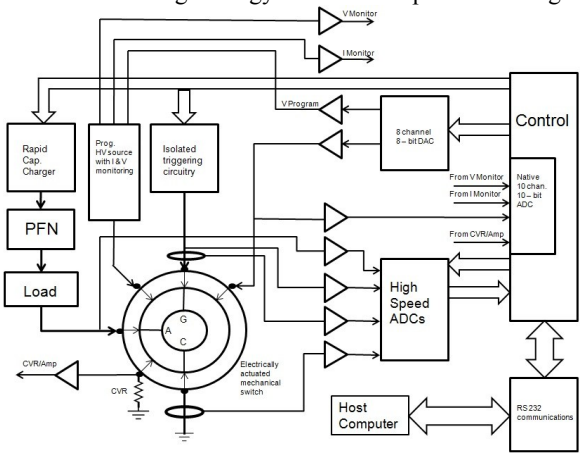

Figure 2. Block Diagram of System

The test bed was designed with a modular approach; while each subsystem acts as a peripheral controlled by the main logic and data acquisition circuitry, each individual subsystem is basically plug – and – play and can simply be altered to suit the particular DUT or application.

A. Pulse Forming Network

Any test bed requires a source of energy to stress the DUT, for the particular devices this system was initially designed for; experimental Si and SiC SGTOs, a Pulse Forming Network (PFN) was designed to achieve repeatable, forced voltage and current levels at set rise and fall times. The specific PFN used is a type Rayleigh line network with maximum voltage and current values of 10kV and 10kA respectively with a pulse width (FWHM) of 100µs and a rise time of 2 kA/µs. Custom capacitors were manufactured by SB electronics while the inductors were made in – house using litz wire to reduce proximity and skin effects. The load was also custom built by HVR at the required 0.5Ω value called for by the PFN and is rated at 550kj. Figure 3 is the PFN and load inside a plexiglass safety shield.

Figure 3. PFN and Load

B. Rapid Capacitor Charger

The rapid capacitor charger developed for this system uses a hard switching H-bridge topology. A square wave PWM signal is produced, fed through a step up transformer and subsequently rectified to finally charge the capacitors in the PFN. A current mode control scheme is used to provide a cascaded feedback network with both inner current loop and outer loop voltage monitoring. The current mode control monitoring provides a nearly constant current source which efficiently charges the PFN capacitors and automatically circumvents potentially dangerous current levels in the case of a short circuit. Fiber optic lines are used to set PFN charge voltage and to read a pulse modulated high voltage monitor while maintaining isolation. This system is able to charge up a capacitor bank in milliseconds and has been documented [3 - 5] to reach repetition rates into the tens of Hz for high voltage (25 kV) charging events. The capacitor charger is rated for 10 kW. This power rating is well above the amount needed to store maximum energy in the PFN. Figure 4 is the complete RCC system including the transformer (immersed in oil).

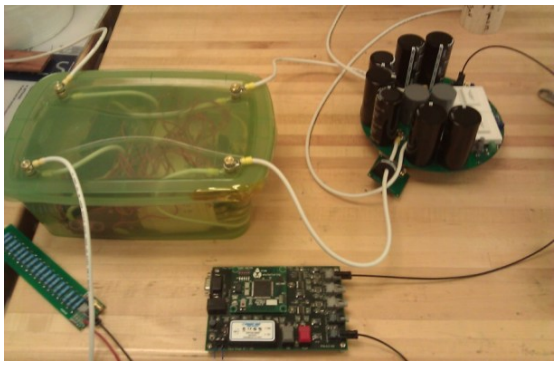

Figure 4. RCC System

C. High – Isolation Electromechanical switch

One of the original design goals of the narrow pulse test bed project was to be able to automatically characterize the devices during test cycles without having to physically remove them from the test bed in order to obtain a progressive record of any changes in the devices parameters for the (known) applied stresses. To achieve this design goal, the DUT must be able to be physically connected to the high power PFN – load path, or a low

power path containing the characterization electronics for IV curve generation with enough electrical isolation to easily withstand the maximum PFN charging voltages while introducing very little resistance or inductance into the PFN – load path. The solution chosen by the P3E engineering team was to design from scratch a custom switch capable of the aforementioned attributes; a rotational three pole double throw electro – pneumatically actuated switch. Figure 5 is a cut – away view of the switch.

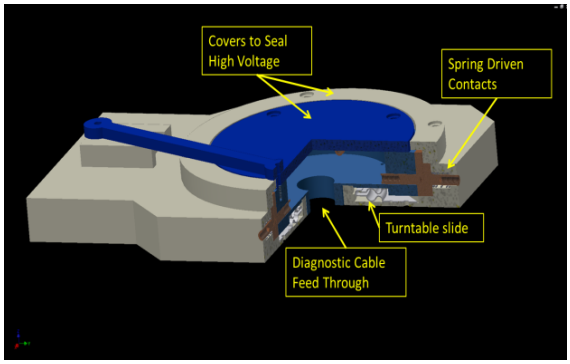

Figure 5. 3PDT High Isolation Switch

The inner rotational section was machined out of DELRIN plastic for its high voltage characteristics while all other plastic parts were generated with the P3E centers 3-D printer. Contacts were machined from copper stock and are a spring loaded design very similar to the brushes in a DC motor. All contacts are kept at a minimal length to reduce inductance and resistance. The high and low power contact sets are separated by a 45° angle. Physical rotation is achieved via a pneumatic piston controlled by an electric valve which is in turn activated by the curve trace module.

D. Fast Characterization Module

To characterize the DUT a curve tracing module was designed and built to acquire a quick, basic I - V set for both the gate and device breakdown in a fraction of the time normally required for such tests. Figure 6 is a picture of the fast characterization peripheral.

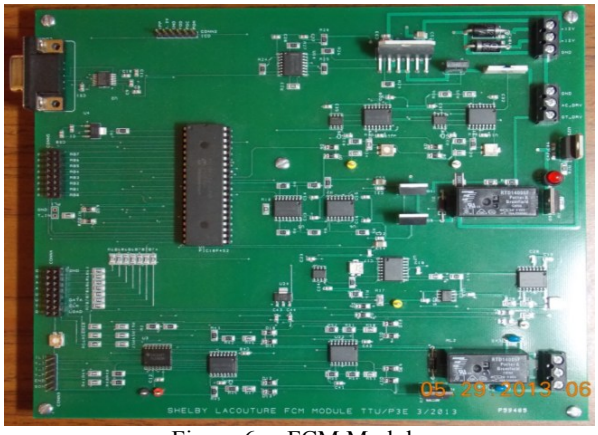

Figure 6. FCM Module

Gate characterization is carried out with a continuous voltage sweep from -10 to +10 volts with current hard limited to approximately 200mA. Currently each complete trace comprised of thirty separate gate voltage and current readings, which are averaged for each of 256 individual points per trace. This compromise between steady readings and time required (Roughly 1 second per trace) was chosen after some experimentation. For high voltage breakdown response of a device, a sweep of 0 to 10kv is completed with current compliance settable from the GUI up to 200µA.

E. Main Control and Logic

Timing and control of each subsystem is orchestrated by a microprocessor – based control module which also serves to acquire test waveforms with several high speed Analog to Digital Converters (ADCs) and on board buffer memory for each separate channel, allowing simultaneous capture of all signals which are uploaded serially during the delay between cycles. Based on user settings received from the host computer the control module sets the PFN charge voltage, initiates ADC conversion and storage, and then triggers the DUT via signals sent through optical cables. This intimate control over every facet of the cycle avoids occurrences such as spurious triggering of a separately attached oscilloscope and makes rep rates possible that could not be approached with a conventional scope due to the time required for data storage – several thousand shots have been performed in a matter of minutes with this test bed, a number that has literally taken days to perform with prior test set ups with conventional equipment attached. Figure 7 shows the main control module connected to the test bed.

Figure 7. Main Control and Acquisition

IV. INITIAL RESULTS

Once the entire system was fully functional, initial testing was carried out using the SiC SGTOs as the DUT. The results of the first battery of testing validated the usefulness of the system both in terms of the ease with which a high volume test cycles can be conducted as well as the efficacy of the system at catching and documenting gradual device failure in the form of I – V characteristic degradation. Figure 8 is a sample saved graph from a single test cycle with the PFN charged to 2.9 kV and discharge current reaching a peak of 2.9 kA. Although each cycle is saved as both raw data and image files, instant feed – back is given through the user GUI.

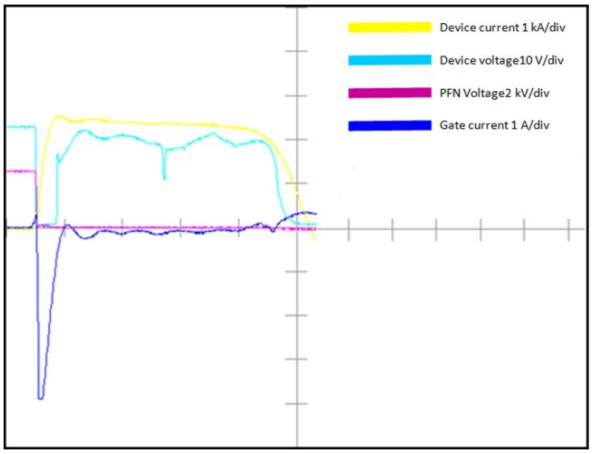

Figure 8. Sample Test Cycle

As stated earlier, an SGTO failure (at conduction levels of approximately 3kA) was documented by the automatic characterization at set intervals; in the final 1000 cycle series run for this particular device, a gate curve trace was set to be carried out every 20 shots, this frequent characterization netted a visual record of the devices slow failure – this was the ultimate goal of the test bed; to capture and record every nuance of failure should it occur during a test. Figure 9 is just a few of the many gate IV traces recorded during the final 1000 shots on the device leading to its ultimate failure.

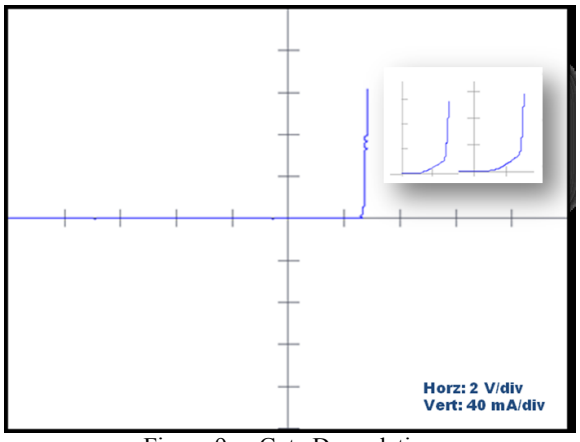

Figure 9. Gate Degradation

V. CONCLUSION

A modular automated testbed with integrated high speed custom diagnostic equipment was designed based on criteria set forth by Army Research Lab at the Center for Pulsed Power and Power Electronics. The system proved itself as a viable research tool during the very first set of testing conducted with SiC SGTO devices, catching not only device failure, but recording a time – line of very gradual changes in the devices characteristics that preceded its breakdown. Knowledge of the specific changes in performance due to the known stresses applied will hopefully aid in understanding of why failure occurred, and lead to improvements in device durability.

VI. REFERENCES

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